REMARKS

Reconsideration of the above-referenced application in view of the amendments and the following remarks is respectfully requested.

Claims 1-11 and 18-26 were pending in this case. Claims 8, 18, 19, 20, 21, 22, 25 have been amended to better define the scope of the claimed invention.

Applicant thanks the Examiner for indicating the allowance of Claim 7.

The drawings were objected to as not showing encapsulant that "does not cover said portion of said sheet metal in said opening coplanar with said second surface of said substrate" or the heatsink or the printed circuit board. Regarding the encapsulant, Figure 1 clearly shows encapsulant 108 that does not cover the bottom surface sheet metal 105b. Note that it is the bottom surface of the sheet metal 105b that is coplanar with the second surface of the substrate. A proposed modification to the drawings is submitted with this paper in order to show the heatsink and printed circuit board described in the instant specification at page 7, lines 13-19 and at page 8, lines 20-22.

Claim 19 stands rejected under 35 U.S.C. 112, second paragraph. The Examiner asserted that Claim 19 is unclear where it states that encapsulant that covers at least a portion of the first surface of the substrate does not cover the second surface of the substrate and does not cover "said portion of said sheet metal in said opening coplanar with said second surface of said substrate." Applicant respectfully points out that the claim refers to first and second surfaces of the substrate which correspond to the top and bottom surface respectively of substrate 101 shown in Figure 1. Encapsulant 108 covers the top surface of the substrate 101 and even a portion of the top surface of sheet metal 105b, but

clearly does not cover the bottom surface of substrate 101 or the bottom surface of sheet metal 105b, which is coplanar with the bottom surface of substrate 101. Applicant believes the claim language to be clear and supported by the specification, including Figure 1.

Claims 1, 2, 4-6 and 18 stand rejected under 35 U.S.C. 102(b) as being anticipated by Johnson (U.S. Patent No. 5,888,849). Applicant respectfully traverses the rejection.

Claim 1 is to a "reel-to-reel tape." Johnson includes the statement "[t]he stiffener makes it possible to handle the flexible film in strips, rolls or small panels" (col. 3, line 5), but does not disclose a reel-to-reel tape. Claim 1 includes the feature of "a chip mount pad, secured to said first surface, coplanar with said second surface." Johnson does not disclose such a chip mount pad. Note that element 10 in Johnson's Figure 6 is a lead, not a mount pad. The clear lack of physical support for chip 6 other than by leads 10 is a likely reason for Johnson's used of encapsulant 16 around the chip and leads. Note further that Johnson uses both the words "pad" (col. 3, line 25) and "leads" (col. 3, line 32) in his disclosure and thus distinguishes those terms. To read Johnson's reference to "leads" as a reference to a mount pad overlooks this distinction. For at least these reasons, Applicant respectfully submits that Claim 1 is patentable over Johnson.

Claim 2 is also to a reel-to-reel tape. As noted above, Johnson does not disclose a reel-to-reel tape. Claim 2 includes the feature of "a chip mount pad in each of said second openings, attached to said first surface and shaped to be coplanar with said second surface." Johnson does not disclose such a chip mount pad. As mentioned above, element 10 in Johnson's Figure 6 is a lead, not a mount pad.

Claim 4 includes the feature "wherein said routing lines and contact lands are created by a photolithographic patterning and chemical etch process." Johnson does not disclose how his circuitry 2 is formed on dielectric 1. Note also

that product-by-process Claim 4 depends from Claim 2, which is patentable over Johnson for the reasons presented above.

Claim 5 includes the feature "wherein said bending of said chip mount pad is provided by a mechanical coining process." Johnson does not disclose a coining process. Note also that product-by-process Claim 5 depends from Claim 2, which is patentable over Johnson for the reasons presented above.

Claim 6 includes the feature "wherein said first and second openings are created by a mechanical punching process." Johnson does not disclose a punching process. Note also that product-by-process Claim 6 depends from Claim 2, which is patentable over Johnson for the reasons presented above.

Claim 18, as amended, includes the feature of "a chip mount pad comprising a sheet of metal, a portion of said sheet of metal on said first surface of said substrate and a portion of said sheet of metal covering said opening such that said portion of said sheet of metal covering said opening is coplanar with said second surface of said substrate, said portion of said sheet of metal covering said opening having first and second opposing surfaces, said second surface of said sheet of metal covering said opening being coplanar with said second surface of said substrate" (see page 7, lines 3 and 4 of the instant specification for support for the amendment). Johnson does not teach or suggest such a feature. Therefore, Applicant submits that Claim 18 is patentable over Johnson.

Claim 3 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson in view of Ikegami (U.S. Patent No. 6,194,781). Applicant respectfully traverses the rejection. Claim 3 depends from Claim 2. As pointed out above, Johnson fails to disclose a chip mount pad as described in Claim 2. Johnson also fails to suggest such a pad. Ikegami does not cure this deficiency of Johnson. Therefore, Applicant submits that Claim 3 is patentable over the cited references.

Claims 8-11 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson in view of Cheng (U.S. Patent Application Publication 2002/0066592). Applicant respectfully traverses the rejection. Claim 8 includes the feature of "a chip mount pad covering each of said second openings, attached to said first surface and shaped to be coplanar with said second surface." As indicated above, Johnson does not teach or suggest such a feature. Cheng does not cure that deficiency of Johnson. Since the combined references fail to teach or suggest all of the claimed features, Applicant respectfully submits that Claim 8 is patentable over the references of record. Claims 9-11 depend from Claim 8 and are therefore patentable over Johnson in view of Cheng for at least the reasons presented above.

Claims 19-24 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson in view of Carter (U.S. Patent No. 5,594,234). Claims 19-21 depend from Claim 18, which, as indicated above, includes features not taught by Johnson. Specifically, Claim 18, as amended, includes the feature of "a chip mount pad comprising a sheet of metal, a portion of said sheet of metal on said first surface of said substrate and a portion of said sheet of metal covering said opening such that said portion of said sheet of metal covering said opening is coplanar with said second surface of said substrate, said portion of said sheet of metal covering said opening having first and second opposing surfaces, said second surface of said sheet of metal covering said opening being coplanar with said second surface of said substrate." As indicated above Johnson does not teach or suggest a mount pad covering an opening in a substrate. Carter does not cure that deficiency of Johnson. Carter's package is a leadframe-based package and thus does not include a substrate. The skilled artisan would therefore receive no motivation from Johnson or Carter to combine Carter's teachings with those of Johnson. Therefore, Applicant submits that Claims 19-21, which depend from Claim 18, are patentable over Johnson in view of Carter.

Claim 22, as amended, includes the feature of "a chip mount pad of metal foil attached to said first surface of said substrate and downset into and covering said opening such that a bottom surface of said chip mount pad is coplanar with said second surface of said substrate." Johnson does not teach or suggest a mount pad downset into and covering an opening in a substrate. Carter does not cure that deficiency of Johnson. Carter's package is a leadframe-based package and thus does not include a substrate. The skilled artisan would therefore receive no motivation from Johnson or Carter to combine Carter's teachings with those of Johnson. Claims 23 and 24 depend from Claim 22 and are therefore patentable over Johnson in view of Carter for at least the reasons presented above.

Claims 25 and 26 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson in view of Cheng and Carter. Claim 25, as amended, includes the feature of "a chip mount pad of metal foil attached to said first surface of said substrate and downset into and covering said opening such that a bottom surface of said chip mount pad is coplanar with said second surface of said substrate." Johnson does not teach or suggest a mount pad downset into and covering an opening in a substrate. Neither Cheng nor Carter cures that deficiency of Johnson. Cheng does not disclose an opening or die mount pad as claimed. Carter's package is a leadframe-based package and thus does not include a substrate. The skilled artisan would therefore receive no motivation from Johnson or Carter or Cheng to combine Carter's teaching with those of Johnson and Cheng. Claim 26 depends from Claim 22 and is therefore patentable over Johnson in view of Carter and Cheng for at least the reasons presented above.

Applicant respectfully requests reconsideration and withdrawal of the rejections and allowance of Claims 1-11 and 18-26. If the Examiner has any questions or other correspondence regarding this application, Applicant requests

that the Examiner contact Applicants' attorney at the below listed telephone number and address.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

Specification:

In the section titled "BRIEF DESCRIPTION OF THE DRAWINGS":

--FIG. 1A [1] is a schematic cross section of a low profile high power ball grid array device as an embodiment of the present invention

FIG. 1B is a schematic cross section of the device of Figure 1A attached to a printed circuit board.

FIG. 1C is a schematic cross section of the device of Figure 1B attached to a printed circuit board including a heatsink.

FIG. 2 is a magnified cross section of a portion of an actual device illustrating key features of the present invention.

FIG. 3A is a magnified top view of a portion of the mounted chip on a substrate fabricated according to the present invention.

FIG. 3B is a highly magnified top view of a portion of the mounted chip on a substrate fabricated according to the present invention.

FIGs. 4 to 12 are schematic and simplified perspective views of plastic tape portions illustrating individual process steps in the fabrication flow of the reel-to-reel tape used in the assembly of the semiconductor devices according to the invention.

FIGs. 13 to 16 are schematic and simplified perspective views of a chip illustrating individual process steps in the assembly and packaging flow of the chip towards a ball grid array type device, as an example of an embodiment of the invention.--

On page 6 of the specification, in the second paragraph:

--In the schematic cross section of FIG. 1A [1], a low profile ball grid array package, generally designated 100, for high power dissipation is shown as an

embodiment of the present invention. The device comprises a plastic tape 101, which has a first surface 101a and a second surface 101b. The first surface 101a is at least partially covered with an adhesive layer (not shown on FIG. 1) so that other materials such as a metal foil can be attached to it. As can be seen in FIG. 1A [1], tape 101 (and the adhesive layer) has a plurality of first openings of diameter 102. These first openings are preferably circular and configured so that each opening can be used for one solder ball 103.—

On page 6 of the specification, in the third paragraph:

--Furthermore, tape 101 has at least one second opening of width 104. This second opening is preferably shaped as a rectangle or a square and has dimensions somewhat larger than the dimensions of the integrated circuit chip 106 of device 100 (more detail in FIG. 2). In the preferred embodiment shown in FIG. 1A [1], there is only one opening of the second kind; it should be pointed out, though, that in other embodiments of the invention, the tape may have two or more openings of the second kind in order to accommodate multi-chip modules.--

On page 6 of the specification, in the fourth paragraph:

--A metal foil 105, preferably copper, is laminated on the adhesive layer covering portions of the first surface 101a of tape 101. As can be seen in FIG. 1A [1], this metal foil 105 covers the first openings of diameter 102 and thus enables the attachment of solder balls 103. A portion of metal foil 105 also covers the second opening of width 104.--

On page 7 of the specification, in the first paragraph:

--It is of pivotal importance for the present invention that the portion 105b of metal foil 105, which overlays the second opening 104, is mechanically shaped (preferably by bending or coining) into a position coplanar with the second

surface 101b of the tape 101. Consequently, a metal foil offset 107 is formed around the periphery of opening 104. It is in this position that the portion 105a of metal foil 105 inside of opening 104 serves as mount pad for the integrated circuit chip 106. The foil portion 105a remains exposed after device 100 is encapsulated by encapsulation material 108, and is thus available for direct attachment to a printed circuit board 150, as shown in Figure 1B. This direct attachment, in turn, minimizes the thermal path, and thus optimizes the heat transport[,] from chip 106 to the printed circuit board and to heat sink 160 as shown in Figure 1C.--

Claims:

8. (twice amended) A low profile, high power semiconductor device including a plastic tape having first and second surfaces, comprising:

a plurality of electrically conductive routing lines and a plurality of contact lands on said first surface, said lands exposed by first openings in said tape;

second openings in said tape configured to accommodate integrated circuit chips;

a chip mount pad covering [in] each of said second openings, attached to said first surface and shaped to be coplanar with said second surface;

a circuit chip mounted by means of a thermally conductive material on each of said chip mount pads;

bonding wires connecting said chip to said contact lands;

encapsulating material surrounding said first tape surface including each of said mounted chips and said wire bonds; and

solder balls attached to each of said exposed lands.

18. (amended) A packaged integrated circuit, comprising:

a substrate having first and second opposing surfaces; said substrate including an opening extending through said substrate from said first surface to said second surface;

a chip mount pad comprising a sheet of metal, a portion of said sheet of metal on said first surface of said substrate and a portion of said sheet of metal covering [in] said opening such that said portion of said sheet of metal covering [in] said opening is coplanar with said second surface of said substrate, said portion of said sheet of metal covering [in] said opening having first and second opposing surfaces, said second surface of said sheet of metal covering [in] said opening being coplanar with said second surface of said substrate;

an integrated circuit chip mounted on said first surface of said sheet of metal in said opening.

19. (amended) The packaged integrated circuit of Claim 18, further comprising encapsulant covering at least a portion of said first surface of said substrate and said chip, wherein said encapsulant does not cover said second surface of said substrate and does not cover said portion of said sheet of metal covering [in] said opening that is coplanar with said second surface of said substrate.

20. (amended) The packaged integrated circuit of Claim 18, further comprising a heatsink attached to said second surface of said sheet of metal covering [in] said opening.

21. (amended) The packaged integrated circuit of Claim 18, wherein said second surface of said sheet of metal covering [in] said opening is attached to a printed circuit board.

22. (amended) A packaged integrated circuit chip, comprising:

a substrate having first and second opposing surfaces; said substrate including an opening extending through said substrate from said first surface to said second surface;

a chip mount pad of metal foil attached to said first surface of said substrate and downset into and covering said opening such that a bottom surface of said chip mount pad is coplanar with said second surface of said substrate;

an integrated circuit chip mounted on a top surface of said chip mount pad;

encapsulation on said first surface of said substrate and not on said second surface of said substrate, such that said encapsulation covers said chip, but does not cover said bottom surface of said chip mount pad.

25. (amended) A packaged integrated circuit chip, comprising:

a substrate having first and second opposing surfaces; said substrate including an opening extending through said substrate from said first surface to said second surface, said opening having a first size;

a plurality of contact lands on said first surface of said substrate adjacent to said opening;

a chip mount pad of metal foil attached to said first surface of said substrate and downset into and covering said opening such that a bottom surface of said chip mount pad is coplanar with said second surface of said substrate;

an integrated circuit chip mounted on a top surface of said chip mount pad, said integrated circuit chip having a second size, wherein said second size is smaller than said first size;

bond wires coupling said integrated circuit chip to said contact lands; and

encapsulation on said first surface of said substrate and not on said second surface of said substrate, such that said encapsulation covers said chip, bond wires, and contact lands, but does not cover said bottom surface of said chip mount pad.